AMENDMENTS TO THE SPECIFICATION

At page 7 please replace the paragraph commencing at line 17 with the following amended paragraph:

FIGS. 3A and 3B include ~~is~~ a flowchart illustrating a method of simultaneously performing data read and write operations using the IC shown in FIG. 2 according to an exemplary embodiment of the present invention;

At page 7 please replace the paragraph commencing at line 20 with the following amended paragraph:

FIG. 4 is a flowchart illustrating process 340 shown in FIG. 3A;

At page 7 please replace the paragraph commencing at line 21 with the following amended paragraph:

FIG. 5 is a flowchart illustrating process 345 shown in FIG. 3A;

At page 7 please replace the paragraph commencing at line 22 with the following amended paragraph:

FIG. 6 is a flowchart illustrating process 355 shown in FIG. 3A;

At page 11 please replace the paragraph commencing at line 15 with the following amended paragraph:

FIGS. 3A and 3B include ~~is~~ a flowchart illustrating a method of simultaneously performing data read and write operations using the IC 200 according to an exemplary embodiment of the present invention. In process 310, it is determined whether both a write address and a read address are input or if the write address or the read address is input during one period of a clock signal. The tag memory controlling unit 210 then receives a write address WADD and a read address RADD via, for example, an input pin

separate from an output pin. If the write address WADD and the read address RADD are input during one period of a clock signal, in process 320, it is determined whether an upper address of the write address WADD is the same as an upper address of the read address RADD.